CLAIMS

1. A circuit comprising:

a first circuit configured to (i) detect a state of an input signal and (ii) present a plurality of intermediate signals each representative of said state of said input signal during a plurality of clock cycles; and

a second circuit configured to present a filtered signal in response to a selected number of said intermediate signals having a predetermined state.

2. The circuit according to claim 1, wherein said first circuit comprises:

a third circuit configured to (i) detect said state of said input signal and (ii) present a detected signal representing said state of said input signal; and

a plurality of shift registers configured to (i) sample said detected signal in each of said clock cycles and (ii) present said intermediate signals.

3. The circuit according to claim 2, wherein said first circuit further comprises a fourth circuit configured to

synchronize said detected signal to a clock signal defining said clock cycles.

4. The circuit according to claim 1, wherein said second circuit comprises:

a plurality of logic gates each configured to present a signal in response to at least two of said intermediate signals; and

a multiplexer configure to multiplex said signals to present said filtered signal.

5. The circuit according to claim 4, wherein each of said logic gates is configured to (i) receive one of said intermediate signals and one of said signals and (ii) present one of said signals.

6. The circuit according to claim 1, further comprising another second circuit configured to present a second filtered signal in response to a second selected number of said intermediate signals having a second predetermined state.

7. The circuit according to claim 6, further comprising a third circuit configured to present a status signal responsive to said filtered signal and said second filtered signal.

8. The circuit according to claim 7, wherein said selected number and said second selected number are programmable.

9. The circuit according to claim 8, wherein said selected number is unequal to said second selected number.

10. The circuit according to claim 9, wherein said predetermined state is a loss-of-signal state and said second predetermined state is a signal present state.

11. A method of filtering an input signal, the method comprising the steps of:

(A) detecting a state of said input signal;

(B) presenting a plurality of intermediate signals each representing said state of said input signal during a plurality of clock cycles; and

(C) presenting a filtered signal in response to a selected number of said intermediate signals having a predetermined state.

12. The method according to claim 11, further comprising the steps of:

presenting a detected signal representative of said state of said input signal in response to detecting; and

sampling said detected signal in each of said clock cycles to present said intermediate signals.

13. The method according to claim 12, further comprising the step of synchronizing said detected signal to a clock signal defining said clock cycles in response to detecting.

14. The method according to claim 11, wherein step C comprises the sub-steps of:

presenting a plurality of signals each in response to at least two of said intermediate signals; and

multiplexing said signals to present said filtered signal.

15. The method according to claim 14, wherein presenting said signals comprises the sub-step of performing a plurality of logical operations each receiving one of said intermediate signals and a one of said signals to present one of said signals.

16. The method according to claim 11, further comprising the step of presenting a second filtered signal in response to a second selected number of said intermediate signals having a second predetermined state.

17. The method according to claim 16, further comprising the step of presenting a status signal responsive to said filtered signal and said second filtered signal.

18. The method according to claim 17, further comprising the step of programming said selected number and said second selected number.

19. The method according to claim 18, wherein said selected number is unequal to said second selected number.

20. A circuit comprising:

means for detecting a state of an input signal;

means for presenting a plurality of intermediate signals each representing said state of said input signal during a plurality of clock cycles; and

means for presenting a filtered signal in response to a selected number of said intermediate signals having a predetermined state.